Docket No. 200207569-1

Amendments to the Drawings:

Replacement sheets for Figure 3 and 4 are submitted herein. In Figure 3, block 330 is amended from "Imaging Mechanism Ready" to read "Imaging Mechanism Ready?" and block 345 is amended from "More Page To Memory" to read "More Pages In Memory". In Figure 4, block 420 is amended from "More Data Pages" to read "More Data Pages?"

PAGE 4/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12

Docket No. 200207569-1

Remarks

This Amendment is responsive to the **June 28, 2007** Office Action. Reexamination and reconsideration of **claims 1-23** is respectfully requested.

Summary of The Office Action

The Drawings were objected to because:

Fig. 3, step 330: it is assumed that applicant intended to cite "Imaging Mechanism Ready?"

Fig. 3, step 345: it is assumed that applicant intended to cite "More Pages in Memory?"

Fig. 4, step 420: it is assumed that applicant intended to cite "More Data Pages?"

The disclosure is objected to because:

Page 5, line 23-24 – it is assumed that applicant intended to cite "Maintaining more data pages within the main memory 150 can decrease processing times..." instead of "Maintaining more data pages within the main memory 150 can increase processing times...".

Claims 1-4, 6-12, 14, 16-23 were rejected under 35 U.S.C. §102(e) as being anticipated by Shishizuka (US Pat. 6,697,898 B1).

Claims 5, 13, 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Shishizuka.

PAGE 10/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12

Docket No. 200207569-1

The Present Amendment

Paragraph [0019] has been amended as pointed out by the examiner. The term "increase" should be "decrease" since the system runs faster and the processing time is less. No new matter has been added.

The Figures 3 and 4 have also been amended as pointed out by the examiner. Replacement Sheets are submitted with this response. No new matter has been added.

I. Claims 1-4, 6-12, 14, 16-23 were rejected under 35 U.S.C. §102(e) as being anticipated by Shishizuka (US Pat. 6,697,898 B1)

35 U.S.C. §102

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach each and every element of the claim. Section 2131 of the MPEP recites:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Independent 1

Claim 1 recites an image forming device comprising a scanner, a memory, a page frame buffer, an imaging mechanism, and a dual bus system with a specific configuration. Shishizuka fails to anticipate the claimed image forming device for the following reasons.

The Office Action cites the "DoEngine" of Shishizuka as teaching the claimed dual bus system. Claim 1 recites the dual bus system as:

> "a dual bus system configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the page of data from the page frame buffer to the imaging mechanism."

PAGE 11/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12

Docket No. 200207569-1

As recited, there are two data transmission paths formed by the dual bus system: image data can be transmitted (1) from the scanner to the memory simultaneously with transmitting the page of data (2) from the page frame buffer to the imaging mechanism.

Looking to the DoEngine taught by Shishizuka (which is best seen in Figure 4), the Office Action cites the two buses, the G bus 404 and the B bus 405. However, the DoEngine fails to teach the claimed configuration. The G bus 404 transmits data between the scanner controller 4302 to the cache memory 403 (via system bus bridge 402), and the B bus transmits data from the cache memory 403 to the printer controller 4303 (via system bus bridge 402). A page frame buffer (being a separate element from the cache memory 403) is not present and not part of the G bus and B bus configuration. Thus, the claimed page frame buffer and the claimed configuration with the recited dual bus system is not taught by Shishizuka.

Applicants notes that the Office Action cites the page memory 511 from Fig. 111 as teaching the claimed page frame memory and cites the RAM 203a from Fig. 108 as teaching the claimed memory. However, these features appear to come from different embodiments and Shishizuka fails to teach the claimed configuration. For example, the RAM 203a in Fig. 108 is connected to a system bus 108, but this fails to teach a particular connection or operation with the G bus 404 or B bus 405, which is relied upon as teaching the dual bus system. Furthermore, the page memory 511 from Fig. 111 is simply shown with block diagram connection lines to the scanner 510 and the printer 512. No separate bus systems are illustrated and Applicant finds no discussion in the cited sections that teach the page memory 511 connected to the G bus 404 or B bus 405 in the claimed manner. Additionally, claim 1 recites that "a page frame buffer configured to store a page of data, copied from the memory." This feature is not taught by the cited sections.

Applicant further notes that the Office Action on page 5 (end of first paragraph) states:

> The "Page Memory 511" in Fig. 111 is contained within "RAM 203a".

PAGE 12/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12

No citation to support this statement was given. Applicant respectfully fails to find such a disclosure in Shishizuka. The examiner is invited to provide a citation, otherwise the statement should be withdrawn as incorrect and Shishizuka should be re-evaluated for its proper teachings.

Based on a number of deficiencies, Shishizuka fails to teach each and every element of claim 1 and fails to establish a prima facie anticipation rejection. The rejection is improper and should be withdrawn. Accordingly, the rejections of dependent claims 2-10 are also improper and should be withdrawn.

Dependent Claim 2

Claim 2 depends from claim 1 and recites that the dual bus system includes a first bus configured to communicate data between the scanner and the memory, and a second bus configured to communicate data between the page frame memory and the imaging mechanism. In view of the discussion of Shishizuka above, Shishizuka fails to teach this configuration of buses. The G bus and B bus from the DoEngine do not have the recited configurations between a scanner and a memory, and between a page frame memory and an imaging mechanism (that operate in parallel transmissions as recited in claim 1). Thus, Shishizuka fails to teach these elements and fails to establish a prima facie anticipation rejection. The rejection should be withdrawn.

Independent Claim 11

The Office Action cites Shishizuka Fig. 111, Page Memory 511 as purportedly teaching the claimed element of "copying a first image data page into a page frame memory from the memory to prepare for imaging" (Office Action, page 8). However, Fig. 111 is a system diagram and thus does not teach a method per se. Furthermore, Fig. 111 does not show a memory block and thus does not show a memory from which image data is copied to

PAGE 13/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12

the Page Memory 511. Therefore, the cited section of Shishizuka fails to support the rejection.

The Office Action cites Shishizuka col. 73, lines 22-34 and Figs. 4, 91 and 108 as purportedly teaching the claimed "transmitting" element. Although Shishizuka provides a generic statement of transmitting data in parallel, it fails to teach the actual claim limitations. Generic references to parallel data transmission is not sufficient to anticipate specific data transmissions between specific components as claimed. Therefore, the cited sections of Shishizuka fails to support the rejection.

Shishizuka fails to establish a prima facie anticipation rejection and the rejection should be withdrawn. Accordingly, the rejections of dependent claims 12-16 are also improper and should be withdrawn.

Independent Claim 17

Independent claim 17 recites a system for formatting image data for an image forming device, comprising "a second data bus configured to communicate the page of data from the second memory to an imaging mechanism where the page of data can be transmitted to the imaging mechanism in parallel with the first memory receiving the image data pages." The Office Action at pages 8-9 alleges that Shishizuka teaches this claimed feature at Figure 4, B Bus 405. However, this cited reference fails to teach the second data bus of claim 17 or the claimed configuration with the first data bus and first memory.

The Office Action cites SDRAM controller 403 (which controls the cache memory) from Fig. 4 as purportedly teaching the claimed first memory, and also RAM 203a from Fig. 108 (Office Action page 10). Applicant notes that Shishizuka does not define the particular connections between RAM 203a and the buses of DoEngine 400 (Fig. 4) and thus RAM 203a does not support an anticipation rejection. Thus, only the cache memory from Fig. 4 is potentially relevant to the rejection. (Applicant will refer to the cache memory as 403 since it is not separately labeled in Fig. 4).

PAGE 14/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12

Then the Office Action cites the B bus 405 from Fig. 4 as teaching the claimed second data bus. However, the B bus 405 also receives data from the same cache memory 403 as the first bus (G bus 404), not from a different second memory "configured to load a page of data that is to be imaged, the page of data being received from the first memory" as recited in claim 17. The Office Action relies upon Shishizuka's Page Memory 511 from Fig. 111 however, no disclosure is provided as to its connections and data communications with the buses of the DoEngine 400 or other memory components. Indeed, Page Memory 511 is part of a different embodiment.

As such, Shishizuka fails to establish a prima facie anticipation rejection due to a number of deficiencies and the rejection is improper. Accordingly, the rejections of dependent claims 18-23 are also improper and should be withdrawn.

II. Claims 5, 13, 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Shishizuka

Claims 5, 13, and 15 are dependent claims. Since the rejection of their independent claim has been shown to be unsupported and improper, then the rejection of the dependent claims is also improper. Shishizuka fails to establish a prima facie anticipation rejection of any claim thus it cannot establish a prima facie obviousness rejection. The rejections should be withdrawn.

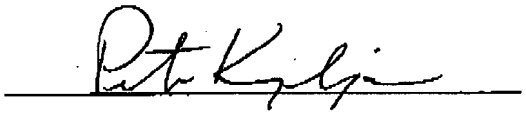
PAGE 15/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12

Docket No. 200207569-1

Conclusion

For the reasons set forth above, **claims 1-23** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,



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PAGE 16/18 * RCVD AT 9/28/2007 12:54:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/19 * DNIS:2738300 * CSID:216 348 5474 * DURATION (mm-ss):02-12